

# Power-take-off topology comparison for a wave energy converter

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**Abstract:** Wave Energy Converters (WECs) generally use a Mechanical Power-Take-Off (MPTO) involving hydraulics or gearing to optimise the extraction of energy from the incoming waves before converting it into electrical energy via a high speed rotating generator. This simplifies the design of the Electrical Power Conversion System (EPCS). Further, it facilitates the use of mechanical energy storage such as hydraulic accumulators to reduce the peaky nature of the power flow and allows the WEC resonant frequency to be tuned for maximum energy capture. This work compares two power electronic converter topologies for an Electrical PTO (EPTO). This EPTO is intended to replace the aforementioned MPTO and generator with a Permanent Magnet Linear Machine (PMLM) directly coupled to the WEC. The compared topologies comprise either a Current Source Converter (CSC) or a Voltage Source Converter (VSC) as the generator interface working in combination with a DC-DC converter and an Energy Storage System (ESS). The principle differences between the two topologies are explored and losses are evaluated in a modular EPCS working with a WEC. Wide-bandgap power electronic switches are assumed for both topologies over a range of switching frequencies. The evaluation concludes that the CSC topology is advantageous at higher switching frequencies.

## 1 Introduction

Replacing the mechanical power-take-off (MPTO) in a wave energy converter (WEC) is the underlying objective of E-Drive. The idea is to replace the MPTO with a direct-drive electrical solution, an electrical direct-drive PTO (EPTO), which is capable of reducing the naturally peaky nature of the WEC power flow and also to tune the natural resonant frequency of the WEC, thus, maximising energy capture by the use of reactive power control [1].

For the EPTO, a generator capable of producing high force at low speeds is required. Given the natural oscillatory and largely linear motion of a heaving WEC, various PMLM topologies are being evaluated elsewhere in this project [2]. From the perspective of the power electronic converter, the most important factors are the magnitudes of generator terminal voltages and currents as well as their time varying nature when operating with the WEC. For reactive power control, the EPCS must operate in all four quadrants and incorporate significant energy storage. The force applied by the generator on the WEC is a combination of the time-varying real and reactive mechanical vectors which typically have an operating frequency of  $\ll 1$  Hz. The relatively short time constants of the converter compared with the WEC indicate that the converter KVA requirements are:

$$KVA_{\text{converter}} = \frac{\sqrt{Pm_{\text{real}}^2 + Pm_{\text{reactive}}^2}}{\eta_g \cdot \cos\phi_g} \quad (1)$$

where  $Pm_{\text{real}}$  and  $Pm_{\text{reactive}}$  are the combination of real and reactive components resulting in maximum mechanical power demand to or

from the WEC,  $\eta_g$  is the generator efficiency and  $\cos\phi_g$  is the generator power factor.

The maximum generator voltage and current are governed by the peak force and velocity applied to the translator and WEC and the specific generator design. For the purposes of this comparison, Table 1 summarises the generator variables used to evaluate the two converter topologies. Under optimal control, the phase current vector is aligned with the generator emf vector for maximum power transfer.

## 2 Converter topologies

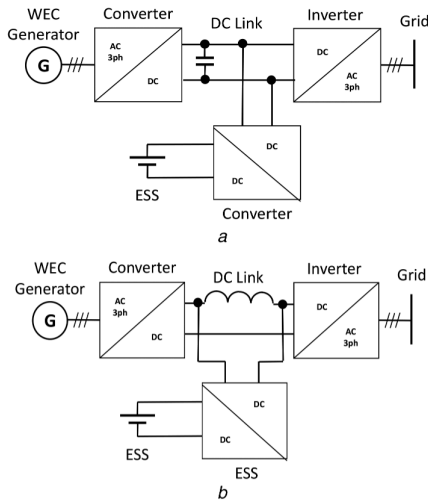
For the concept EPTO, a modular approach has been proposed whereby multiple PMLM sections are mechanically coupled and connected to multiple EPCS modules [3]. A single module of the EPCS is illustrated in Fig. 1 for both a current source and voltage source topology. The important elements of each module are the generator converter, the ESS interface and the grid inverter. The ESS, using supercapacitors, permits the dynamic exchange of mechanical energy during reactive power control of the WEC and also to smooth the fluctuating real power through the grid interface. In this comparison, the grid interface inverter is replaced with a simple controlled resistive load and the comparison focuses on the behaviour of the generator interface and ESS DC-DC converters.

The chosen power electronic topologies for this study are presented in Fig. 2 for the VSC and Fig. 3 for the CSC. For the VSC topology, a three-phase converter is employed with an AC low pass filter to mitigate the impact of high  $dv/dt$  on the generator cable and machine windings. It is assumed the DC link is maintained at a constant value based on the generator voltage specification. The ESS requires a bi-directional DC-DC converter

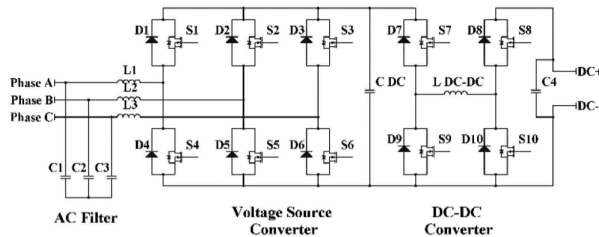
**Table 1** Generator parameters

Parameter	Value	Parameter	Value
$xg@50$ Hz	$j25.13 \Omega$	Vph	234 V
rg	0.7 $\Omega$	Iph	8.1 A
emf@50 Hz	121 V	Pmax	2750 W

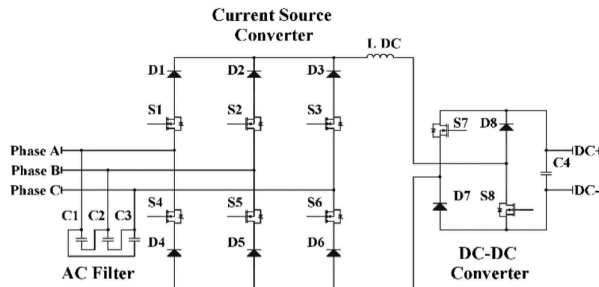




**Fig. 1** One E-drive EPCS module  
(a) – VSC. (b) – CSC



**Fig. 2** VSC topology



**Fig. 3** CSC topology

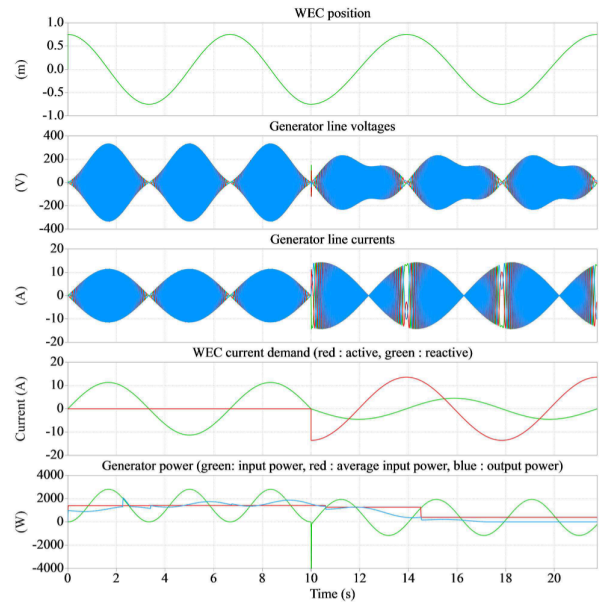
to achieve the desired voltage control. For the CSC topology, the commutation capacitors already provide a high degree of  $dv/dt$  reduction to the generator and cabling. The current to voltage DC-DC conversion for the ESS is a fundamental part of the chosen CSC topology [3].

### 2.1 Converter operation on a WEC

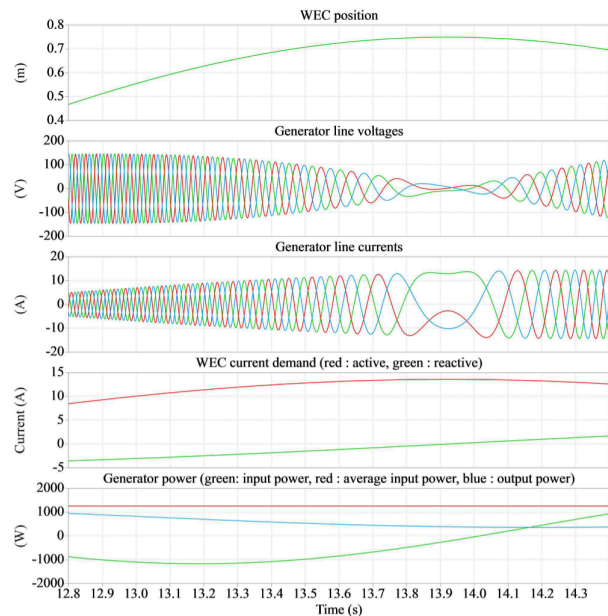
For the comparison, both converters are modelled under two distinct WEC operating conditions. The first is where the incoming regular waves are at the same frequency as the resonant frequency,  $\omega_{nat}$ , of the WEC. i.e.  $\omega_{nat} = \omega_{wave} = 0.942$  rad/sec. This is the condition for maximum power transfer to the grid; the ESS is now solely used to level the power flow from the WEC.

The second condition is when the WEC is operating off resonance, i.e.  $\omega_{nat} > \omega_{wave}$ ,  $\omega_{wave} = 0.801$  rad/sec. In this case mechanical reactive power is being applied and returned from the WEC to achieve reactive power flow. The available real power is reduced and in this specific case the generator current increases. From a generator and converter perspective, increasing the mechanical reactive power will necessarily reduce the maximum real power, even if the WEC could produce it.

The magnitude of the generator and converter current is limited by design. For illustration, a selection of generator variables are



**Fig. 4** WEC operation [ $t_{0s} - t_{10s}$  ( $\omega_{wave} = 0.942$  rad/sec) &  $t_{10s} - t_{22s}$  ( $\omega_{wave} = 0.801$  rad/sec)]



**Fig. 5** Generator waveforms with reactive power control ( $\omega_{wave} = 0.801$  rad/sec)

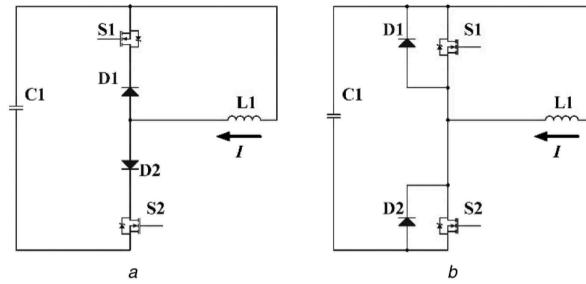
presented for both operating conditions in Fig. 4 and in expanded view in Fig. 5. The associated power flows are summarised in Table 2.

### 3 Switching losses in the VSC and CSC

To ensure a fair comparison, both converters have been analysed using the same Silicon Carbide (SiC) MOSFET (Rohm SCT3030KL) and SiC Schottky diodes (Rohm SCS240KE2) devices. In the VSC topology, the MOSFET's internal diode is bypassed by the SCS240KE2 diode and in the CSC topology, the MOSFET is connected in series with the SCS240KE2 diode to create a reverse blocking switch. These particular devices are not optimised for the chosen power ratings or topologies, but being 1200 V devices rated for a continuous forward current of at least 40A provide a sensible voltage and current margin for this investigation and future experimental validation.

**Table 2** Converter test conditions

Parameter	$\omega = 0.942$ (rad/sec)	Parameter	$\omega = 0.801$ (rad/sec)
pg (rms)	1939 W	Pg (rms)	1183 W
pg (pk)	2800 W	Pg (pk)	1935 W
pg (mean)	1413 W	Pg (mean)	392 W



**Fig. 6** VSC and CSC commutation test circuits

Analysis of switching losses in converters is routinely carried out during the design phase based on prior knowledge of the input and output waveforms with assumptions relating to the thermal environment and gate control circuit behaviour. Equations (2)–(5) are typically adopted to estimate the conduction and switching losses [4].  $P_c^{FET}$  and  $P_c^{Diode}$  are conduction losses for the MOSFET and diode, respectively,  $E_{sw}^{FET}$  is the switching energy during any MOSFET switching event and in turn is a function of  $V_v, I_v$  before the event and  $V_v, I_v$  after the event. Finally, diode switching losses in a SiC diode are related to the charge stored in the junction capacitance.

$$P_c^{FET} = V_{ds,o} * i_v + i_v^2 r_{DS(on)} \quad (2)$$

$$P_c^{Diode} = V_{f,o} * i_v + i_v^2 r_{f(on)} \quad (3)$$

$$E_{sw}^{FET} = E_{on} * \frac{I_v}{I_{ref}} * \frac{V_v}{V_{ref}} + E_{off} * \frac{I_v}{I_{ref}} * \frac{V_v}{V_{ref}} \quad (4)$$

$$E_{sw}^{Diode} = Q_c * \frac{V_v}{2} \quad (5)$$

Differences exist in the distribution and processes for switching losses in the CSC and VSC. For example, the reverse recovery energy of antiparallel diodes in the VSC is usually assumed to be dissipated in MOSFETs in the associated leg, whereas in the CSC it may be dissipated elsewhere in the converter. Zero voltage switching (ZVS) and zero current switching (ZCS) conditions exist in the CSC depending on the switching state and load conditions resulting in reduced switching losses compared with a VSC [5].

A further complication relates to the third quadrant operation of MOSFETs. For example, in a VSC with an inductive load, the incoming MOSFET will conduct reverse current instead of the antiparallel diode if the gate is energised and the magnitude of the current is such that the MOSFET on-state voltage is less than the forward conduction voltage of the diode [6].

For this study, PLEXIM® has been applied. Device switching is based on ideal models for both the MOSFETs and diodes with switching and conduction losses calculated according to (2) and (3) at each time step and (4) and (5) when a switching event is detected. Test scenarios were created to verify the underlying calculations based on commutation test circuits of Fig. 6. Steady-state conditions can be enforced by making C1 and L1 large and setting the initial conditions accordingly.

By way of example, a single switching event is illustrated in Fig. 7 for both test circuits. Initial conditions are the same in both cases i.e.  $I_{L1} = 27A$ . For the CSC, the voltage on C1 is  $-565V$ . The FET gates signals must overlap, FET 1 is switched on before FET 2 switches off. In this case the current is forced through FET1 as diode 2 blocks. For the VSC, the voltage on C1 is  $+650V$ . In

this case the FET gate signals must not overlap during changeover and FET 1 is switched off before FET 2 is switched on. During this dead-time, diode D1 carries the inductor current. Once FET 1 is on, it now carries reverse current in preference to the antiparallel diode as its on-state voltage is lower than that of the forward biased diode.

Under steady-state test conditions, as defined above, the switching and conduction losses are plotted against switching frequency in Fig. 8.

As expected, conduction losses dominate at low switching frequencies for both converters. Comparing total losses in Fig. 9, the VSC has the lowest combined loss at low switching frequencies with the CSC having lower combined losses above 100kHz.

Clearly, this simplified approach is ignoring a number of important factors such as the increasing relevance of parasitic losses and gate drive losses which can increase errors, especially at high switching frequencies.

#### 4 VSC and CSC topologies compared

This comparison focuses on the main loss mechanisms in the two topologies under the two operating conditions identified earlier, i.e.  $\omega_{wave} = 0.801$  rad/sec and  $\omega_{wave} = 0.942$  rad/sec. The capacity of the ESS is the same in both topologies and the control is designed to measure and dissipate the average real power from the WEC in a resistive load.

Examples of significant operational parameters for each topology are presented in Figs. 10 and 11. Here we can see that the power flows, the ESS State of Charge (SOC) and the generator phase current are the same for each topology. A key difference is the nature of the DC link control:

- For the VSC, the DC-Link is held at 690 V with the ESS voltage entirely controlled by the DC-DC converter.
- For the CSC, acknowledging that the WEC does not require very high dynamic performance, thus, the DC-Link inductor current is controlled to just exceed the magnitude of current demanded by the generator current controller. This approach goes some way to reduce the conduction losses and will significantly improve efficiency of the CSC at lower power. The DC-DC converter and CSC work together to control both the ESS voltage and DC link current.

Conduction and switching losses for the main elements in the two topologies are presented in Figs. 12 and 13 for the  $\omega_{wave} = 0.942$  rad/sec operating condition over a range of switching frequencies from 10 up to 200 kHz.

These are the mean values measured during the maximum power flow from the WEC i.e. at 2800 W. The converter current flows are essentially constant regardless of the device switching frequencies; hence, the elements that reflect conduction losses are

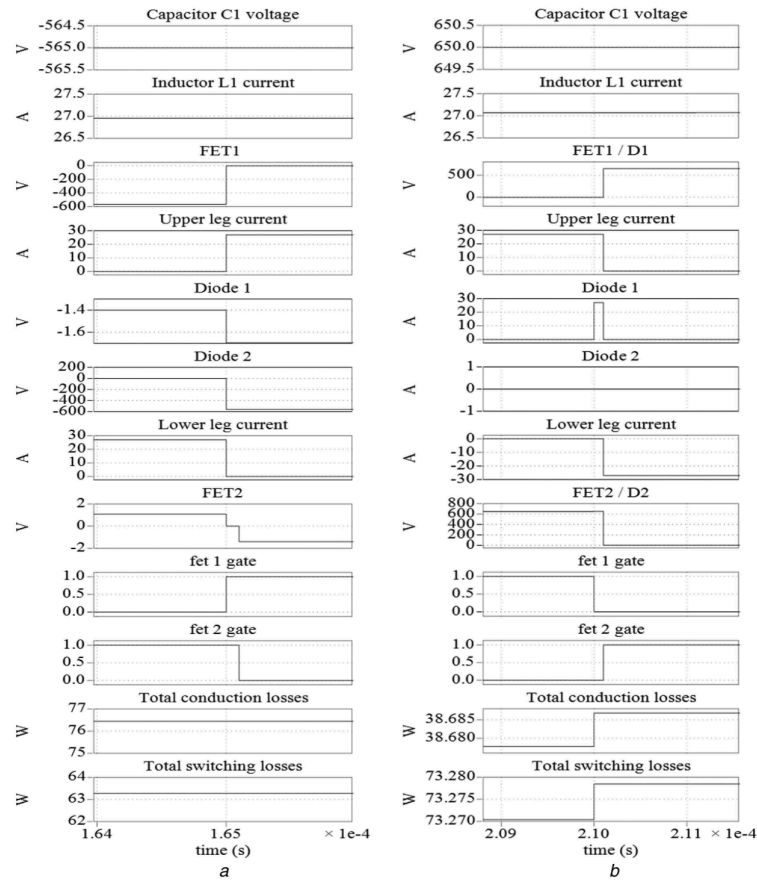


Fig. 7 Example switching (a) CSC, (b) VSC

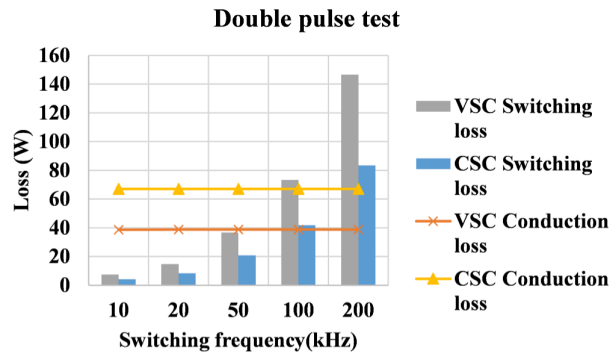


Fig. 8 VSC and CSC commutation test results

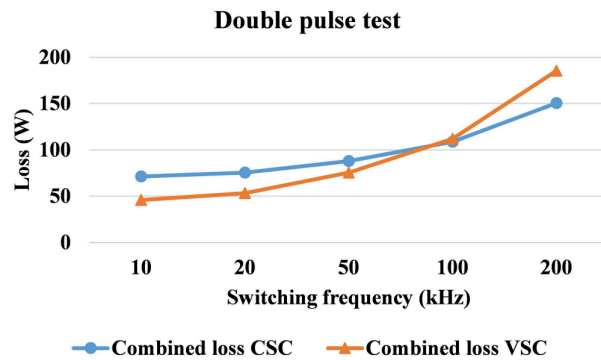


Fig. 9 Comparing losses under steady-state

largely unchanged over the switching frequency range. As before, we can see that the switching losses dominate in the VSC at higher

switching frequencies and conduction losses dominate in the CSC at lower switching frequencies.

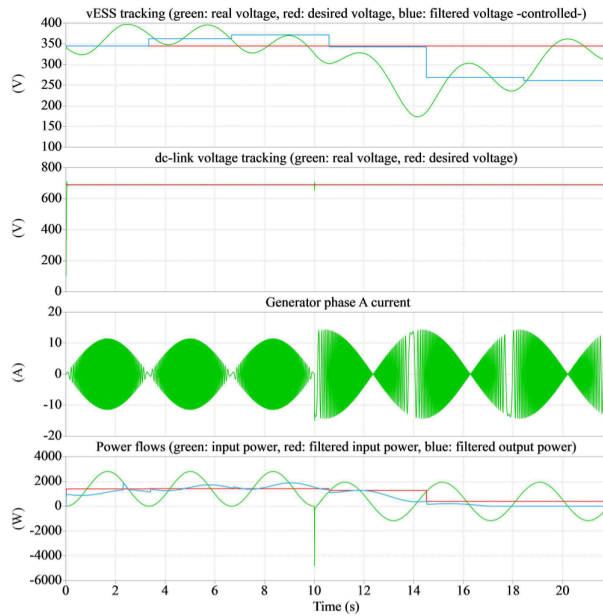


Fig. 10 VSC operation

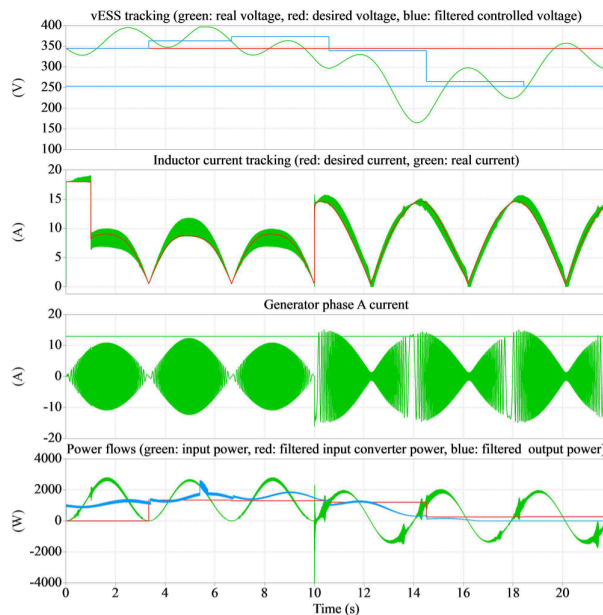


Fig. 11 CSC operation

If we now consider the total losses both over a full WEC period and not just at WEC peak power flow for both converters as in Figs. 14 and 15 it is possible to determine where the optimum switching frequencies are for each topology.

Under optimum WEC operation, the CSC topology operating with a switching frequency of  $> 40$  kHz dominates in terms of operating efficiency. However, when operating away from resonance, where the magnitude of the generator current is somewhat higher, the switching frequency needs to be  $> 65$  kHz for the CSC to dominate.

## 5 Discussion

Reduction in the size of passive components and losses in power electronics is an ongoing aim for converter designers. SiC devices with their lower switching and conduction losses are an enabler for this aim. Increasing the switching frequency will reduce the energy storage requirements for either DC-link capacitors or inductors in the CSC or VSC, respectively and in turn reduce the cost and

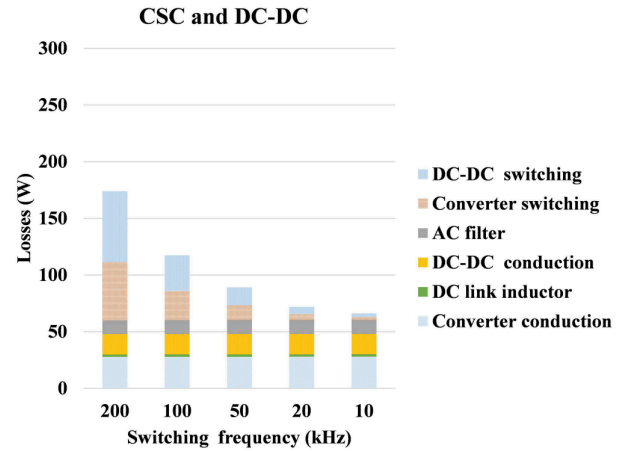


Fig. 12 CSC system losses at  $\omega_{wave} = 0.942$  rad/sec

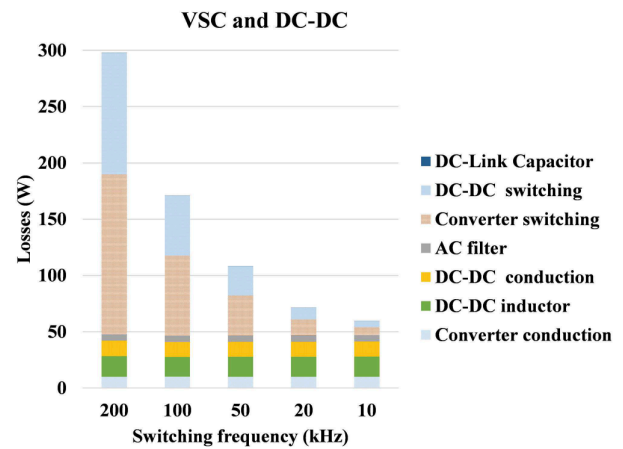


Fig. 13 VSC system losses at  $\omega_{wave} = 0.942$  rad/sec

volume as illustrated by Table 3 which is based on manufacturer's data acquired for this project.

The analysis presented here, provides some insight into the potential benefit of adopting a CSC based topology compared to the more conventional VSC based topology for this WEC application, but only if it can be operated with a high switching frequency. The primary weaknesses of any CSC based topology tends to be higher conduction losses, resonance due to the commutation filter capacitors and perhaps a more challenging layout if parasitic inductances are to be avoided. In part, this is due to the lack of an established 'industry standard' for the CSC and a lack of optimised reverse blocking SiC switches.

The conduction losses issue has been partially addressed here for a WEC application by adopting DC-link current modulation. Dynamic response will still be quite reasonable in a CSC with such a high switching frequency and certainly good enough for a WEC. Commutation capacitor resonance has been noted in the simulations and will need to be further addressed within the control development in due course. Active damping is typically incorporated to mitigate this resonance which can be triggered by harmonics in the generator and/or converter output frequency.

There remain a number of areas for more detailed investigation such as comparing the switching device utilisation factors for the two converters and a incorporating a better understanding of parasitic losses. The loss mechanism within the main passive components has been much simplified in this analysis and will need to be revised in due course. However, although the proportion of the losses within the passive components may change, it seems unlikely they will deviate sufficiently to disturb the general observed behaviour of main the loss making elements, i.e. the switching devices.

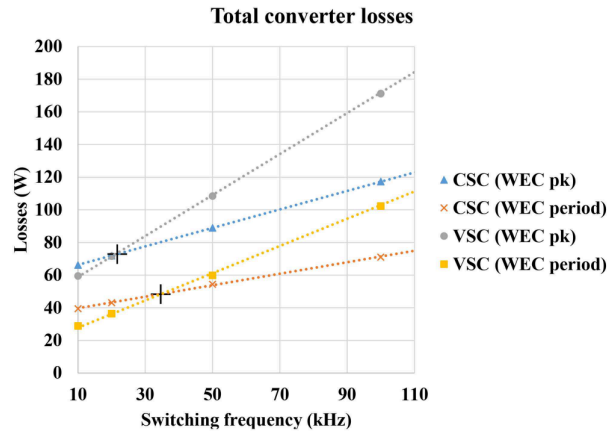


Fig. 14 Converter loss at  $\omega_{wave} = 0.942$  rad/sec

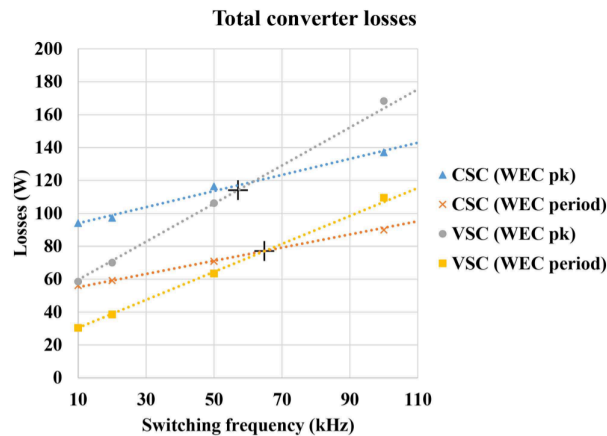


Fig. 15 Converter loss  $\omega_{wave} = 0.801$  rad/sec

Table 3 DC link inductor

Switching frequency	Required inductance	Cost	Volume
5 kHz	10 mH	£1375	0.0365 m <sup>3</sup>
10 kHz	5 mH	£985	0.0304 m <sup>3</sup>
100 kHz	0.5 mH	£420	0.0023 m <sup>3</sup>

## 6 Conclusion

A CSC based topology has been compared with a VSC based topology for a direct-drive WEC application. The basis of this comparison is to evaluate the switching and conduction losses in the main switching and passive elements when operating at two representative states of the associated WEC and generator. The study concludes that for lower switching frequencies, i.e. < 30–40 kHz, the VSC topology is more efficient but at higher switching frequencies, i.e. > 40–65 kHz the CSC is more efficient. A higher switching frequency will result in significant reductions in passive component dimensions and costs for either topology.

## 7 Acknowledgments

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## 8 References

- [1] Shek, J.K.H., Macpherson, D.E., Mueller, M.A.: 'Power conversion for wave energy applications', in, Power Electronics, Machines and Drives (PEMD 2010), 5th IET Int. Conf. on, Brighton, UK, 2010
- [2] Baker, N.J., Raihan, M.A.H., Almoraya, A.A., *et al.*: 'Electric machine design for wave energy converters', in, European Wave and Tidal Energy Conf. - EWTEC2017, Cork, Ireland, 2017
- [3] McDonald, S.P., Pickert, V., Baker, N.: 'High-Efficiency current-source converter for All-electric wave energy conversion systems', European Wave and Tidal Energy Conf., Cork, Ireland, 2017
- [4] Mohr, M., Fuchs, F.W.: 'Comparison of three phase current source inverters and voltage source inverters linked with Dc to Dc boost converters for fuel cell generation systems', in, 2005 European Conf. on Power Electronics and Applications, Dresden, Germany, 2005
- [5] Avery, C.R., Burrow, S.G., Mellor, P.H.: 'Comparison of losses in igt based voltage and current source converters using a single switching pole approach', in, 5th IET Int. Conf. on Power Electronics, Machines and Drives (IET PEMD, 2010), Brighton, UK, 2010
- [6] Callanan, R., Rice, J., Palmour, J.: 'Third quadrant behavior of Sic mosfets', in, 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), Long Beach, CA, USA, 2013